描述 / Descriptions

BRCD6522SE is a wide input voltage, high efficiency Active CC step-down DC/DC converter that operates in either CV(Constant Output Voltage) mode or CC(Constant Output Current) mode.

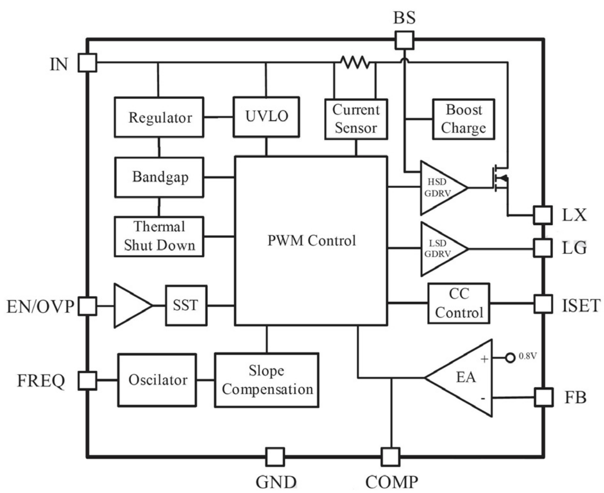
特征 / Features

- 42V Input Voltage Surge
- Wide input voltage:9~37V
- Up to 5A Output Current
- Integrated 50mΩ Power MOS
- Output Voltage up to 12V
- 185kHz Switching Frequency
- ±6.5% CC Accuracy
- – Compensation of Input /Output Voltage Change
- – Independent of inductance and Inductor DCR
- 2% Feedback Voltage Accuracy
- Advanced Feature Set
- – Integrated Soft Start
- – Thermal Shutdown
- – UVLO
- – OVP
- – Secondary Cycle-by-Cycle Current Limit
- Protection Against Shorted ISET Pin

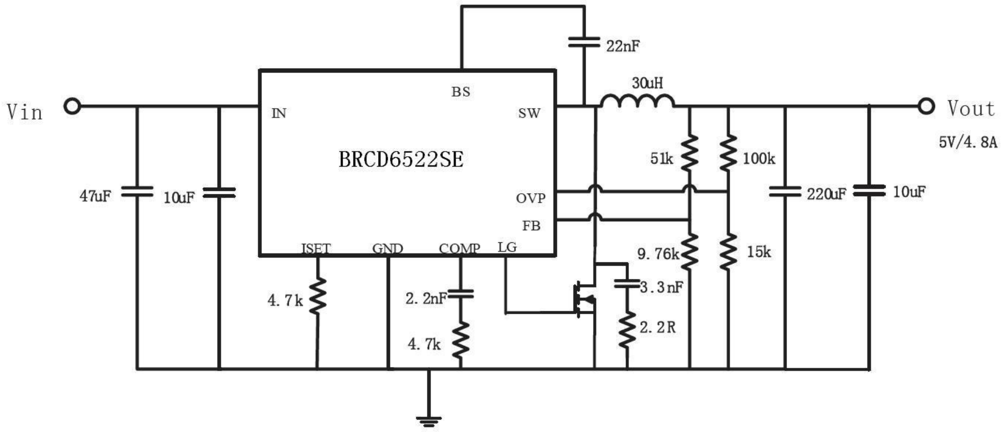
用途 / Applications

- Car Charger/ Adaptor
- Rechargeable Portable Devices
- General-Purpose CC/CV Supply

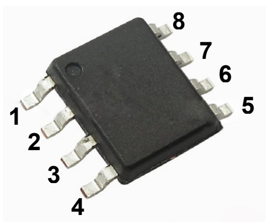
内部等效电路 / Equivalent Circuit

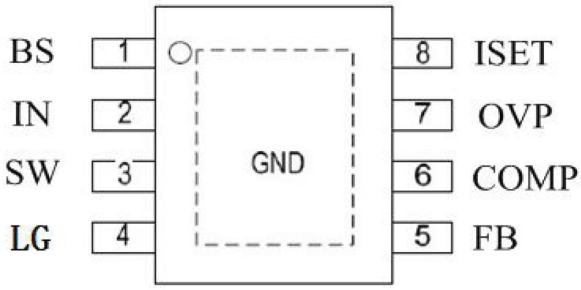


典型应用 / Typical Application



引脚排列 / Pinning





PIN	NAME	FUNCTION
1	BS	High side Gate Driver bias pin, Provide supply to high-side nLDMOS Gate Driver. Connect a 22nF capacitor between BS and SW
2	IN	Power Input pin
3	SW	Switching Pin, Connect to external Inductor
4	LG	Low Side power MOS Drive pin
5	FB	Feedback pin
6	COMP	EA Compensation pin
7	OVP	Over-Voltage Protect pin
8	ISET	Limit Current set pin

印章代码 / Marking

见印章说明。See Marking Instructions.

极限参数 / Absolute Maximum Ratings(Ta=25℃)

参数 Parameter	数值 Rating	单位 Unit
Voltage Range(IN,SW)	-0.3 to 42	V
Voltage Range(BS to SW)	-0.3 to 6.0	V
Voltage Range (All Pins)	-0.3 to 6.0	V
Junction Temperature	-40 ~+150	℃
Storage Temperature	-50~+150	℃
Package Thermal Resistance	46	℃/W
VESD(Human Body Model for all pins)	±2000	V

电性能参数 / (V_{IN}=12V, V_{OUT}=5.0V, T_A = 25°C, unless otherwise noted.)

参数 Parameter	符号 Symbol	测试条件 Test Conditions	最小值 Min	典型值 Typ	最大值 Max	单位 Unit
Input Voltage Range	V_{IN}		9.0		37	V
Input Voltage Surge	V_{INS}				42	V
Under Voltage Lockout	V_{UVLO}	Vin rising		8.2		V
UVLO Hysteresis	$V_{UVLO-HY}$			1.0		V
Input Supply Current	I_{IN}	no load ,VFB>0.83V		1.0		mA
Feedback Threshold Voltage	V_{FBTH}		784	800	816	mV
FB Pin input current	I_{FB}		-50		50	nA
OVP Threshold voltage	V_{OVPTH}	OVP rising		800		mV
Soft start Time	T_{SST}			400		μS
Current limit cycle-by-cycle	$I_{LIM-MAX}$	Duty=0.5		7.5		A
SW leakage	$I_{SW-LEAK}$				10	μA
ISET Voltage	V_{ISET}			1.0		V
ISET Current Gain	G_{ISET}	IOUT/ISET, RISET =12K		29K		A/A
Switch On-Resistance (high side)	R_{DSONH}			50		mΩ
Oscillator Frequency	F_{OSC}	VFB=0.8V		185		kHZ
Short circuit Frequency	F_{SC}	VFB=0V		40		kHZ
Minimum Turn-on Time	T_{ON-MIN}			200		nS
Maximum Duty-cycle	D_{MAX}			85		%
Thermal Shutdown Threshold	T_{SDN}			155		℃
Thermal Shutdown Hysteresis	T_{SDN-HY}			20		℃

功能描述 / Functional Description

CV/CC Loop Regulation

As seen in Functional Block Diagram, the BRCD6522SE is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to VSW + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.8V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 185kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 40kHz at VFB =0.15V.

Over Voltage Protection

The BRCD6522SE has an OVP pin. If the voltage at this pin exceeds 0.8V, the IC shuts down high side switch.

Thermal Shutdown

The BRCD6522SE disables switching when its junction temperature exceeds 155℃ and resumes when the temperature has dropped by 20℃

应用信息 / Application Information

Output Voltage Setting

Figure 1:
Output Voltage Setting

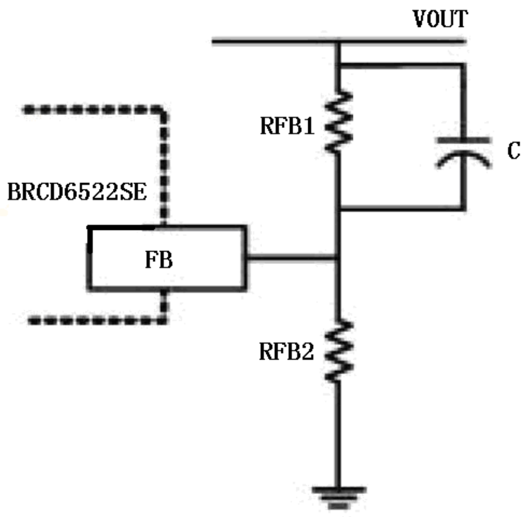
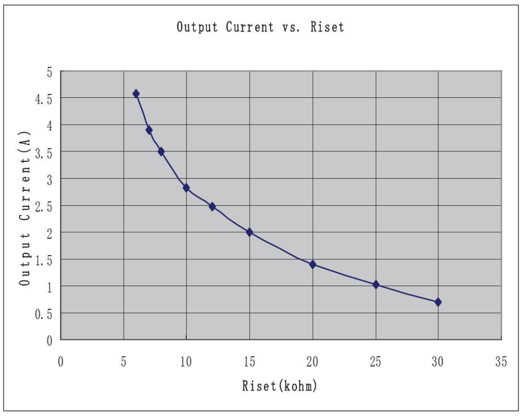


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with RFB1 helps the system stability. Typically, use RFB2 ≈10kΩ and determine R_{FB1} from the following equation:$R_{FB1}=R_{FB2}(V_{OUT} / 0.8V-1)$

CC Current Setting

BRCD6522SE constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1.1V and the current gain from ISET to output is roughly 29000 (29mA/1μA). To determine the proper resistor for a desired current, please refer to Figure 2 below.

Figure 2:
Curve for Programming Output CC Current



应用信息 / Application Information

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:
dependent on the inductance value:
Higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L=V_{OUT}(V_{IN}-V_{OUT})/(V_{IN}f_{SW}I_{LOADMAX}KR_{IPPLE})$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak–to- peak ripple current being 30% of the maximum load current.
With a selected inductor value the peak-to- peak inductor current is estimated as:

$$I_{LPKPK}=V_{OUT}(V_{IN}-V_{OUT})/(LV_{IN}f_{SW})$$

The peak inductor current is estimated as:

$$I_{LPK}=I_{LOADMAX}+1/2I_{LPKPK}$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

$$I_{OUTMAX}=I_{LIM}-1/2\ I_{LPKPK}$$

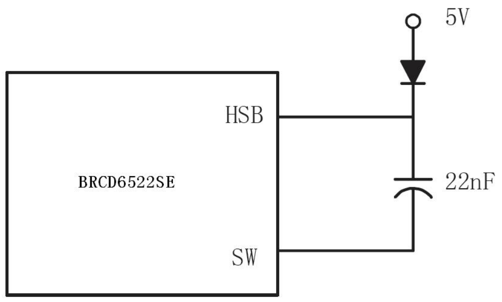
L_{LIM} is the internal current limit, which is typically 6.5A, as shown in Electrical Characteristics Table.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.

Figure 3:

External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

应用信息 / Application Information

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.
The input capacitance needs to be higher than10uF. The best choice is the ceramic type, tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1uF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE}=I_{OUTMAX}K_{LPKPK}R_{ESR}+V_{IN}/(27f_{sw}^{2}LC_{OUT})$$

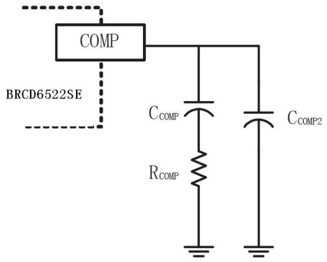
Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.
For ceramic output capacitor, typically choose a capacitance of about 22uF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

应用信息 / Application Information

Figure 4:
Stability Compensation



The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 4. The DC loop gain of the system is determined by the following equation:

$A_{VDC}=0.8V / (I_{OUT} \times A_{VEA} G_{COMP})$

The dominant pole P1 is due to C_{COMP}:$f_{P1}=G_{EA} / (2\pi A_{VEA} G_{COMP})$

The second pole P2 is the output pole: $f_{P2}=G_{EA} / (2\pi V_{OUT} C_{OUT})$

The first zero Z1 is due to R_{COMP} and C_{COMP}: $f_{Z1}=1 / (2\pi R_{COMP} C_{COMP})$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used): $f_{P3}=1 / (2\pi R_{COMP} C_{COMP2})$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$R_{COMP}=2\pi V_{OUT} C_{OUT} f_{SW} / (10 G_{EA} G_{COMP} \times 0.8V)=4.1\times10^7 V_{OUT} C_{OUT}$

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15kΩ,the equation for C_{COMP} is: $C_{COMP}=2.83\times10^5 / R_{COMP}$

If R_{COMP} is limited to 15kΩ, then the actual cross over frequency is 6.58 / ($V_{OUT} C_{OUT}$).

Therefore:$C_{COMP}=6.45\times10^{-6} V_{OUT} C_{OUT}$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:$R_{ESRCOUT} \geqslant \{\text{Min } 1.77\times10^{-6} / C_{OUT}, 0.006\times V_{OUT}\}$

And the proper value for C_{COMP2} is: $C_{COMP2}= C_{OUT} R_{ESRCOUT} / R_{COMP}$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

Table 1:
Typical Compensation for Different Output Voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	C_{COMP}	C_{COMP2}
2.5V	47μF	5.6KΩ	2.2nF	None
3.3V	47μF	6.2 KΩ	2.2nF	None
5.0V	47μF	12 KΩ	2.2nF	None
2.5V	220μF/30mΩ	20 KΩ	2.2nF	47pF
3.3V	220μF/30mΩ	20 KΩ	2.2nF	47pF
2.5V	220μF/30mΩ	20 KΩ	2.2nF	47pF

应用信息 / Application Information

CC Loop Stability

The constant-current control loop is internally compensated over the 1500 mA -3000mA output range. No additional external compensation is required to stabilize the CC current.

Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the BRCD6522SE integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin. Use the curve in Figure 5 to choose the proper feedback resistance values for cable compensation. R_{FB1} is the high side resistor of voltage divider. In the case of high R_{FB1} used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 6, adding a capacitor in paralleled with R_{FB1} or increasing the compensation capacitance at COMP pin helps the system stability.

Figure 5:

Cable Compensation at Various Resistor Divider Values

Typical R_{FB1} is 51k for cable compensation.

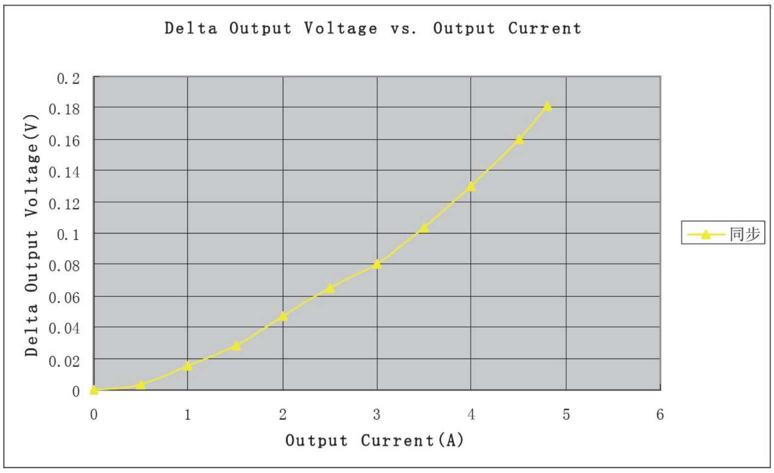
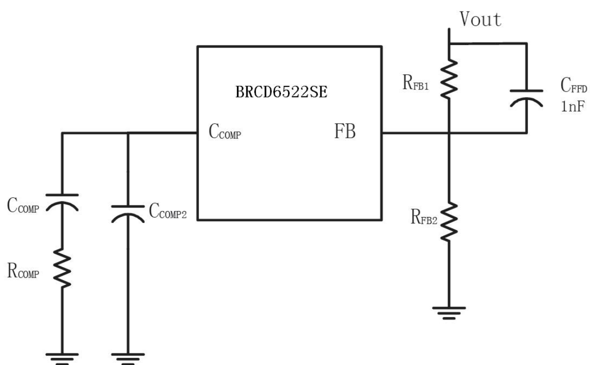


Figure 6:

Frequency Compensation for High R_{FB1}



PC Board Layout Guidance

When laying out the printed circuit board, the Following checklist should be used to ensure proper operation of the IC.

1) Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin and the schottky diode.

2) Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.

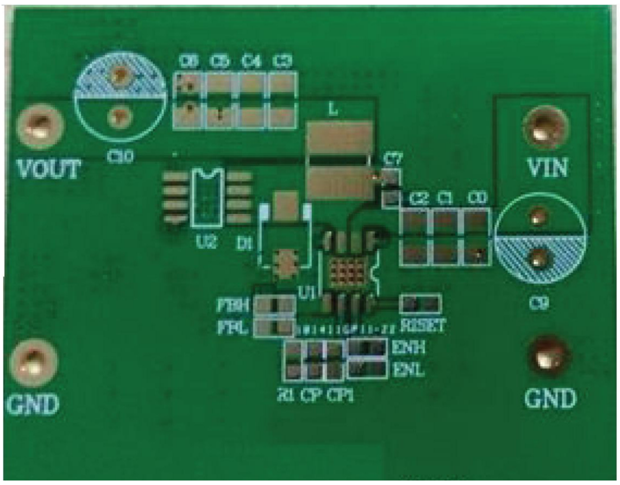
3) Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.

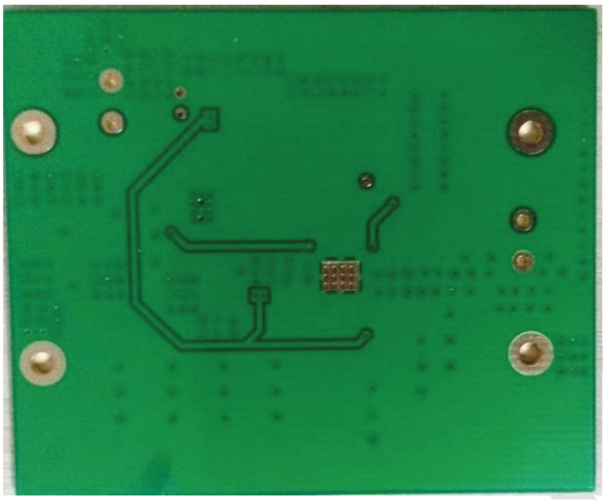
4) Use copper plane for power GND for best heat dissipation and noise immunity.

5) Place feedback resistor close to FB pin.

6) Use short trace connecting HSB-CHSB-SW loop

Figure 7: PCB Layout





应用信息 / Application Information

Figure 8: Typical Application Circuit for 5V/4.8A Car Charger

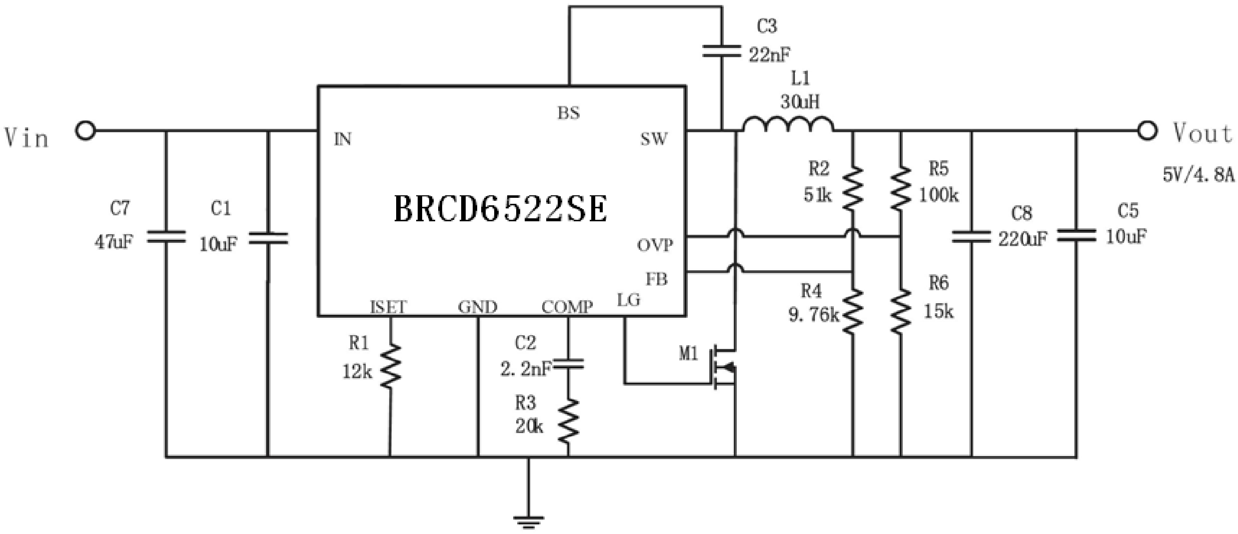
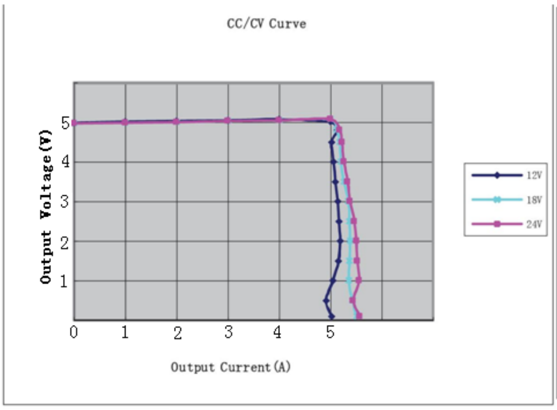


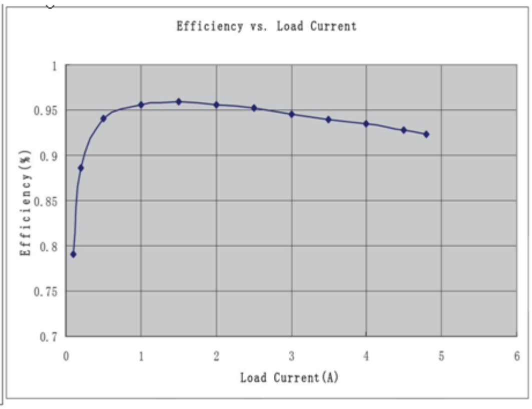
Table 2: BOM List for 5V/2.4A Car Charger

ITEM	REFERENCE	DESCRIPTION	QTY
1	U1	IC, BRCD6522SE, ESOP-8	1
2	C1	Capacitor, Ceramic, 10uF/50V, 1206, SMD 6.3*7mm	1
3	C2	Capacitor, Ceramic, 2.2nF/6.3V, 0603,SMD	1
4	C3	Capacitor, Ceramic, 22nF/50V, 1206,SMD	1
5	C5	Capacitor, Ceramic, 10uF/10V, 0603,SMD	1
6	C7	Capacitor, Electrolytic, 47uF/50V	1
7	C8	Capacitor, Electrolytic, 220uF/10V,6.3*7mm	1
8	L1	Inductor, 30uH,5A, 20%, SMD	1
9	M1	NMOS	1
10	R1	Chip Resistor,12kΩ, 0603,1%	1
11	R2	Chip Resistor, 51kΩ, 0603,1%	1
12	R3	Chip Resistor, 20kΩ,0603,1%	1
13	R4	Chip Resistor,9.76kΩ,0603,1%	1
14	R5	Chip Resistor,100kΩ,0603,1%	1
15	R6	Chip Resistor,15kΩ,0603,1%	1

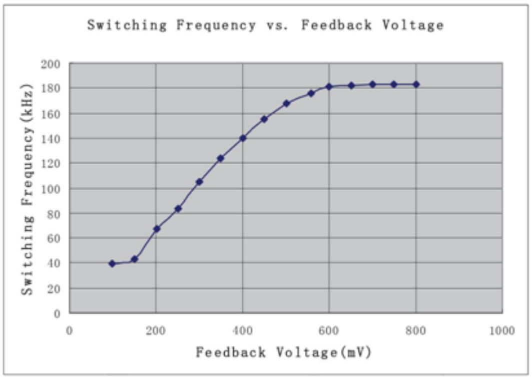
典型性能特征 / Typical Performance Characteristics

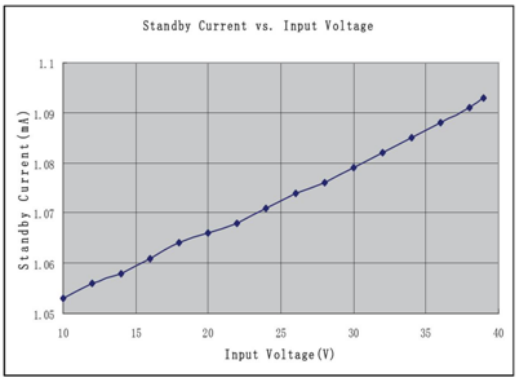


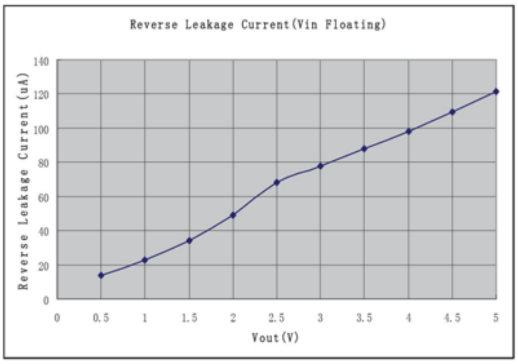
Output: 5V

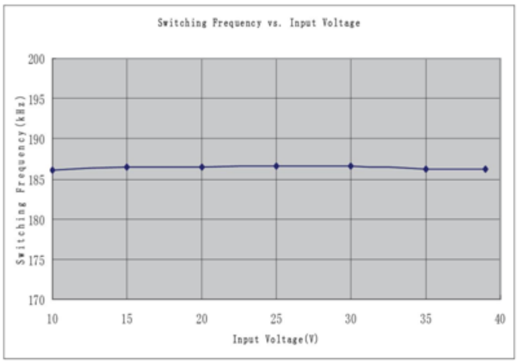


Output: 5V

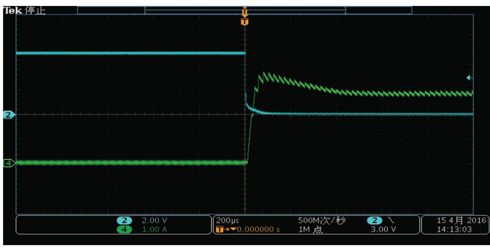






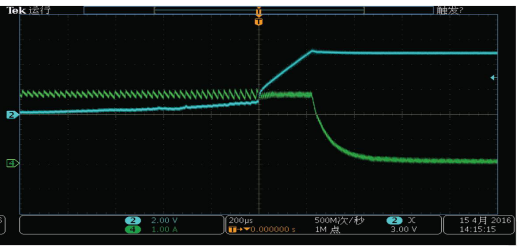


Short Circuit



CH2:Vout,2V/div
CH4:Iout,1A/div
TIME:200us/div

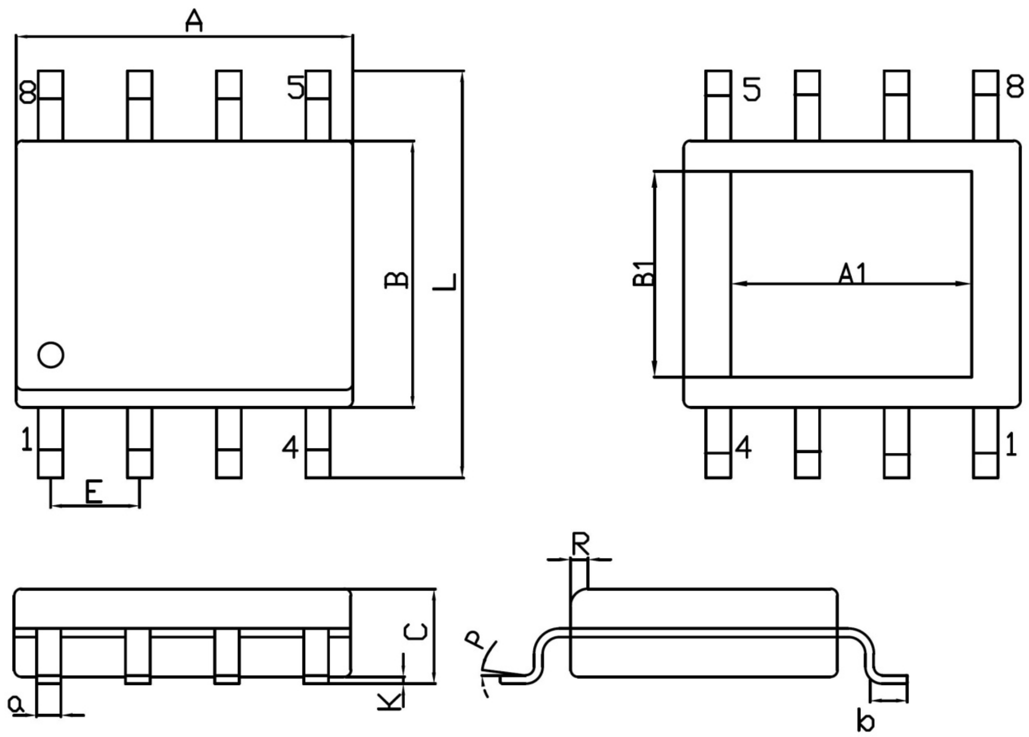
Short Circuit Recovery



CH2:Vout,2V/div
CH4:Iout,1A/div
TIME:200us/div

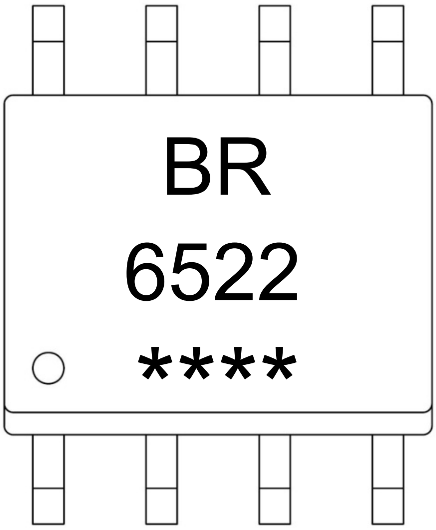
外形尺寸图 / Package Dimensions

ESOP-8 Unit:mm



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.35	1.75
B	3.70	4.10	a	0.35	0.49
L	6.00	6.40	R	0.30	0.60
E	1.27BSC		P	0°	7°
K	0.02	0.10	b	0.40	1.25
A1	3.1	3.5	B1	2.2	2.6

印章说明 / Marking Instructions



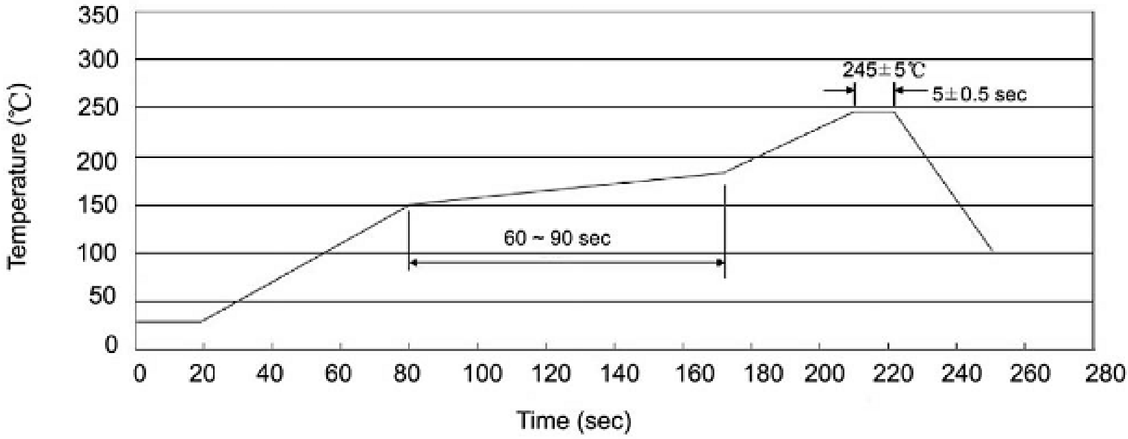
说明：

BR：	为公司代码
6522：	为产品型号
****：	为生产批号代码，随生产批号变化。

Note:

BR:	Company Code.
6522:	Product Type.
****:	Lot No. Code, code change with Lot No.

回流焊温度曲线图(无铅) / Temperature Profile for IR Reflow Soldering(Pb-Free)



说明：
1、预热温度 150～180℃，时间 60～90sec;
2、峰值温度 245±5℃，时间持续为 5±0.5sec;
3、焊接制程冷却速度为 2～10℃/sec.

Note:
1.Preheating:150~180℃, Time:60~90sec.
2.Peak Temp.:245±5℃, Duration:5±0.5sec.
3. Cooling Speed: 2~10℃/sec.

耐焊接热试验条件 / Resistance to Soldering Heat Test Conditions

温度：260±5℃　　时间：10±1 sec.

Temp.:260±5℃　　Time:10±1 sec

包装规格 / Packaging SPEC.

卷盘包装 / REEL

Package Type 封装形式	Units 包装数量					Dimension 包装尺寸 (unit: mm^3)		
	Units/Reel 只/卷盘	Reels/Inner Box 卷盘/盒	Units/Inner Box 只/盒	Inner Boxes/Outer Box 盒/箱	Units/Outer Box 只/箱	Reel	Inner Box 盒	Outer Box 箱
SOP-7/SOP/ESOP-8	4,000	2	8,000	6	48,000	13″ ×16	360×360×50	380×335×366

使用说明 / Notices